



TET ESTEL AS
ESTONIA

**June
2013**

**Series
T173-3200**

**Phase Control Press-Pack
Thyristor
Type T173-3200**

Center amplifying gate
Low on-state and switching losses
Designed for traction and industrial applications

Maximum mean on-state current	I_{TAV}	3200 A
Maximum repetitive peak off-state and reverse voltage	U_{DRM}	400 ÷ 1000 V
Turn-off time	t_q	125; 160; 200; 250 µs
U _{DRM} , U _{RRM} , V	400	500
Voltage code	4	5
Tvj, °C	6	7
	8	9
	10	
	- 60 ÷ 140	

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	T173-3200	Conditions
I _{TAV}	Mean on-state current	A	3200 4980	Tc=95 °C, Tc=55 °C, 180° half-sine wave, 50 Hz
I _{TRMS}	RMS on-state current	A	5024	Tc=95 °C
I _{TSM}	Surge on-state current	kA	65 71	Tvj=140°C Tvj=25°C
I ² t	Limiting load integral	kA ² s	21125 25205	Tvj=140°C Tvj=25°C
U _{DRM} , U _{RRM}	Repetitive peak off-state and reverse voltage	V	400÷1000	Tj min≤Tvj≤Tjm 180° half-sine wave, 50 Hz Gate open
U _{DSM} , U _{RSM}	Non-repetitive peak off-state and reverse voltage	V	500÷1100	Tj min≤Tvj≤Tjm 180° half-sine wave tp=10 ms, Single pulse Gate open
(di _T /dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	400 200	Tvj=140°C ; Ud=0,67 U _{DRM} , Gate pulse : 10V, 5 Ω, 1µs rise time, 10 µs
U _{RGm}	Peak reverse gate voltage	V	5	Tj min≤Tvj≤Tjm
T _{stg}	Storage temperature	°C	-60÷80	
Tvj	Junction temperature	°C	-60÷140	

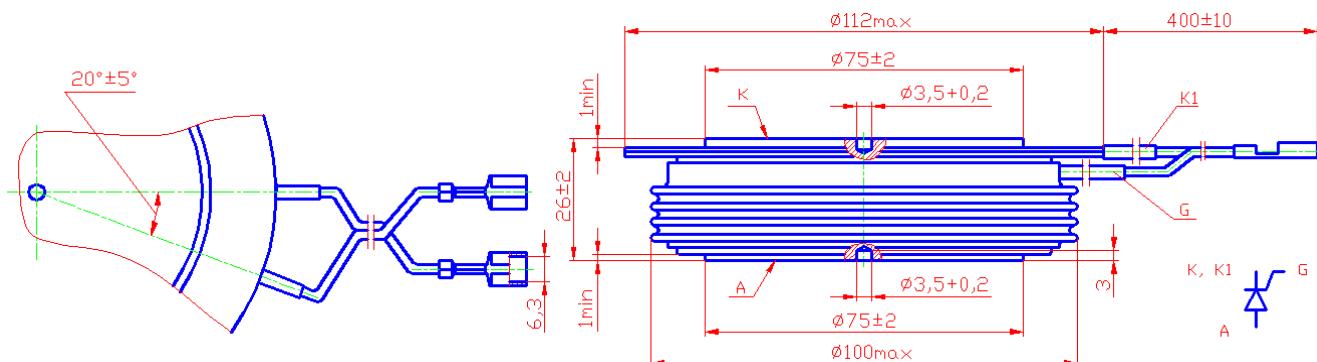
CHARACTERISTICS

U _{TM}	Peak on-state voltage	V	1,5	Tvj=25°C, I _{TM} =3,14 I _{TAV}
U _{T(TO)}	Threshold voltage	V	0,85	Tvj=140°C
R _T	On-state slope resistance	mΩ	0,07	1,57 I _{TAV} < I _T <4,71 I _{TAV}
I _{DRM} I _{RRM}	Repetitive peak off-state and reverse current	mA	200 200	Tvj=140°C, UD = U _{DRM} UR = U _{RRM}

CHARACTERISTICS				
Symbols and parameters		Units	T173-3200	Conditions
I _L	Latching current	A	3,0	Tvj=25°C, UD=12V Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs
I _H	Holding current	A	0,3	Tvj=25°C, UD=12V, Gate open
U _{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C UD=12V
I _{GT}	Gate trigger direct current	A	0,3 0,85	Tvj=25°C, Tvj=-60°C
U _{GD}	Gate non-trigger direct voltage	V	0,35	Tvj=140°C, UD = 0,67 U _{DRM} Direct gate current
I _{GD}	Gate non-trigger direct current	mA	20	
t _{gd}	Delay time	µs	3,2	Tvj=25°C, UD=500V ITM = 3200 A
t _{gt}	Turn-on time	µs	16	Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs
t _q	Turn-off time	µs	125÷250	Tvj=140°C, ITM=3200 A di _R /dt=10 A/µs, U _R =100V UD = 0,67 U _{DRM} du _D /dt=50 V/µs
Q _{rr}	Recovered charge	µC	5000	Tvj=140°C, ITM=3200 A dir/dt=10 A/µs, UR=100V
t _{rr}	Reverse recovery time	µs	27	
I _{RRM}	Peak reverse recovery current	A	370	
(dud/dt)crit	Critical rate of rise of off-state voltage	V/µs	500 1000	
R _{thjc}	Thermal resistance junction to case	°C/W	0,01	Direct current, double side cooled

ORDERING						
	T	173	3200	8	7	3
	1	2	3	4	5	6

1. Phase control thyristor.
2. Design version.
3. Mean on-state current, A.
4. Voltage code (8=800V).
5. Critical rate of rise of off-state voltage ($6 \geq 500 \text{ V/}\mu\text{s}$, $7 \geq 1000 \text{ V/}\mu\text{s}$).
6. Group of turn-off time ($\text{du}_D/\text{dt}=50 \text{ V/}\mu\text{s}$, $2 \leq 250 \mu\text{s}$; $3 \leq 160 \mu\text{s}$; $X2 \leq 125 \mu\text{s}$).



Mounting force : 36 ÷ 46 kN

Weight : 1200 grams