



TET ESTEL AS
ESTONIA

June
2013

Series
T373-2000

Phase Control Press-Pack
Thyristor
Type T373-2000

Center amplifying gate
Low on-state and switching losses
Designed for traction and industrial applications

Maximum mean on-state current	I_{TAV}	2000 A		
Maximum repetitive peak off-state and reverse voltage	U_{DRM}	2000 ÷ 2600 V		
Turn-off time	U_{RRM}	250; 320; 400 μs		
U_{DRM}, U_{RRM}, V	2000	2200	2400	2600
Voltage code	20	22	24	26
$T_{vj}, °C$	- 60 ÷ 125			

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	T373-2000	Conditions
I_{TAV}	Mean on-state current	A	2000 3470	$T_c=94 °C$, $T_c=55 °C$, 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	3140	$T_c=94 °C$
I_{TSM}	Surge on-state current	kA	46 50	$T_{vj}=125 °C$ $T_{vj}=25 °C$ tp=10 ms $U_R=0$
I^2t	Limiting load integral	kA ² s	10580 12500	$T_{vj}=125 °C$ $T_{vj}=25 °C$
U_{DRM}, U_{RRM}	Repetitive peak off-state and reverse voltage	V	2000 ÷ 2600	$T_j \min \leq T_{vj} \leq T_{jM}$ 180° half-sine wave, 50 Hz Gate open
U_{DSM}, U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	2100 ÷ 2700	$T_j \min \leq T_{vj} \leq T_{jM}$ 180° half-sine wave tp=10 ms, Single pulse Gate open
$(di_T/dt)_{crit}$	Critical rate of rise of on-state current : non - repetitive repetitive	A/μs	400 200	$T_{vj}=125 °C$; $U_D=0,67 U_{DRM}$, Gate pulse : 10V, 5 Ω, 1 μs rise time, 10 μs
U_{RGM}	Peak reverse gate voltage	V	5	$T_j \min \leq T_{vj} \leq T_{jM}$
T_{stg}	Storage temperature	°C	-60 ÷ 80	
T_{vj}	Junction temperature	°C	-60 ÷ 125	

CHARACTERISTICS

U_{TM}	Peak on-state voltage	V	1,6	$T_{vj}=25 °C$, $I_{TM}=3,14 I_{TAV}$
$U_{T(TO)}$	Threshold voltage	V	0,9	$T_{vj}=125 °C$
R_T	On-state slope resistance	mΩ	0,13	1,57 $I_{TAV} < I_T < 4,71 I_{TAV}$
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	150 150	$T_{vj}=125 °C$, $U_D = U_{DRM}$ $U_R = U_{RRM}$

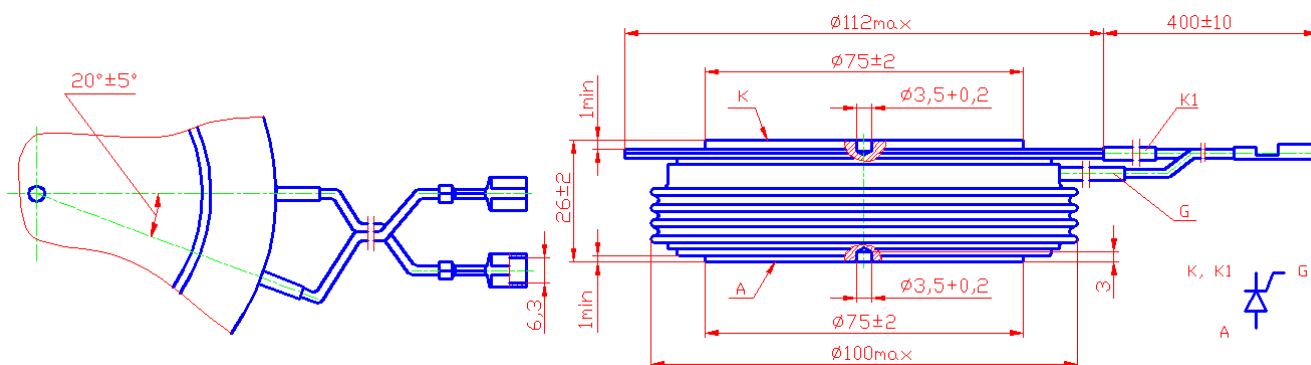
CHARACTERISTICS

Symbols and parameters		Units	T373-2000	Conditions
I_L	Latching current	A	3,0	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$ Gate pulse : 10V, 5 μs , 1 μs rise time, 10 μs
I_H	Holding current	A	0,3	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$, Gate open
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$ $U_D=12\text{V}$
I_{GT}	Gate trigger direct current	A	0,3 0,85	$T_{vj}=25^{\circ}\text{C}$, $T_{vj}=-60^{\circ}\text{C}$
U_{GD}	Gate non-trigger direct voltage	V	0,35	$T_{vj}=125^{\circ}\text{C}$, $U_D = 0,67 U_{DRM}$
I_{GD}	Gate non-trigger direct current	mA	20	Direct gate current
t_{gd}	Delay time	μs	3,2	$T_{vj}=25^{\circ}\text{C}, U_D=500\text{V}$ $I_{TM} = 2000 \text{ A}$
t_{gt}	Turn-on time	μs	16	Gate pulse : 10V, 5 μs , 1 μs rise time, 10 μs
t_q	Turn-off time	μs	250÷400	$T_{vj}=125^{\circ}\text{C}$, $I_{TM}=2000 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}$, $U_R=100\text{V}$ $U_D = 0,67 U_{DRM}$ $du_D/dt=50 \text{ V}/\mu\text{s}$
Q_{rr}	Recovered charge	μC	4500	$T_{vj}=125^{\circ}\text{C}$, $I_{TM}=2000 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}$, $U_R=100\text{V}$
t_{rr}	Reverse recovery time	μs	40	
I_{rrm}	Peak reverse recovery current	A	225	
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	V/ μs	500 1000	$T_{vj}=125^{\circ}\text{C}$, $U_D = 0,67 U_{DRM}$ Gate open
R_{thjc}	Thermal resistance junction to case	$^{\circ}\text{C}/\text{W}$	0,01	Direct current, double side cooled

ORDERING

	T	373	2000	24	7	2	
	1	2	3	4	5	6	

- Phase control thyristor.
- Design version.
- Mean on-state current, A.
- Voltage code (24=2400 V).
- Critical rate of rise of off-state voltage ($6 \geq 500 \text{ V}/\mu\text{s}$, $7 \geq 1000 \text{ V}/\mu\text{s}$).
- Group of turn-off time ($du_D/dt=50 \text{ V}/\mu\text{s}$, $H_2 \leq 400 \mu\text{s}$; $K_2 \leq 320 \mu\text{s}$; $2 \leq 250 \mu\text{s}$).



Mounting force : 36 ÷ 46 kN
Weight : 1200 grams