	TET ESTEL AS ESTONIA	**June 2013**

Series
TFI133S-400

High Frequency Inverter grade Capsule Thyristor Type TFI133S-400

Strong distributed amplified gate
and low turn-off time thyristor for
high frequency applications to 20 kHz

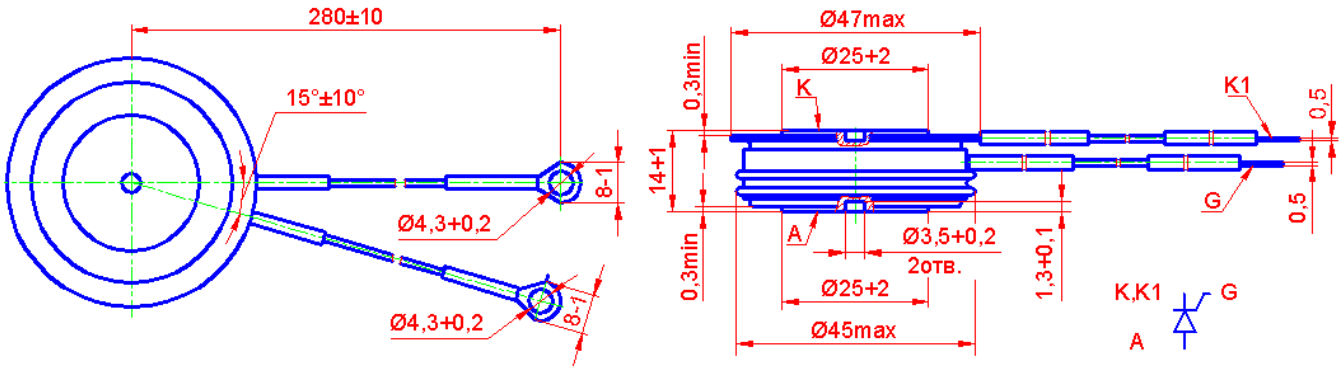
Maximum mean on-state current				I_{TAV}	**400 A**		
Maximum repetitive peak off-state and reverse voltage				U_{DRM} U_{RRM}	**600 ÷1200 V**		
Turn-off time				**tq**	**5; 6,3 µs**		
U_{DRM}, U_{RRM}, V	600	700	800	900	1000	1100	1200
Voltage code	6	7	8	9	10	11	12
Tvj, °C	- 60 ÷ 125						

MAXIMUM ALLOWABLE RATINGS					
Symbols and parameters		Units	TFI133S-400	Conditions	
I_{TAV}	Mean on-state current	A	400 560	Tc=81 °C, Tc=55 °C, 180° half-sine wave, 50 Hz	
I_{TRMS}	RMS on-state current	A	628	Tc=81 °C	
I_{TSM}	Surge on-state current	kA	6,5 7,0	Tvj=125°C Tvj=25°C	tp=10 ms U_R=0
I^2t	Limiting load integral	kA^2s	211 245	Tvj=125°C Tvj=25°C	
U_{DRM},U_{RRM}	Repetitive peak off-state and reverse voltage	V	600÷1200	Tj min≤Tvj≤Tjм 180° half-sine wave, 50 Hz Gate open	
U_{DSM},U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	660÷1300	Tj min≤Tvj≤Tjм 180° half-sine wave tp=10 ms, Single pulse Gate open	
(di$_T$/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/µs	 1600 1000	Tvj=125°C ; U_D=0,67 U_{DRM}, Gate pulse : 10V,5 Ω, 1µs rise time, 10 µs	
U_{RGM}	Peak reverse gate voltage	V	5	Tj min≤Tvj≤Tjм	
Tstg	Storage temperature	°C	-60÷80		
Tvj	Junction temperature	°C	-60÷125		
CHARACTERISTICS					
U_{TM}	Peak on-state voltage	V	3,0	Tvj=25°C, I_{TM}=3,14 I_{TAV}	
$U_{T(TO)}$	Threshold voltage	V	1,8	Tvj=125°C 1,57 I_{TAV}< I_T <4,71 I_{TAV}	
R_T	On-state slope resistance	mΩ	0,95		
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	50 50	Tvj=125°C, U_D = U_{DRM} U_R= U_{RRM}	

CHARACTERISTICS					
Symbols and parameters		Units	TFI133S-400	Conditions	
I_L	Latching current	A	12	Tvj=25°C,U_D=12V Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs	
I_H	Holding current	A	0,5	Tvj=25°C,U_D=12V, Gate open	
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	Tvj=25°C, Tvj=-60°C	U_D=12V
I_{GT}	Gate trigger direct current	A	0,4 0,9	Tvj=25°C, Tvj=-60°C	
U_{GD}	Gate non-trigger direct voltage	V	0,25	Tvj=125°C, U_D = 0,67 U_{DRM} Direct gate current	
I_{GD}	Gate non-trigger direct current	mA	10		
tgd	Delay time	µs	1,6	Tvj=25°C,U_D=500V I_{TM} = 400 A Gate pulse : 10V, 5Ω, 1 µs rise time, 10µs	
tgt	Turn-on time	µs	2,5		
tq	Turn-off time	µs	5,0 ; 6,3 6,3 ; 8,0	Tvj=125°C, I_{TM}=400 A di_R/dt =10 A/µs, U_R=100V U_D = 0,67 U_{DRM} du_D/dt=50 V/µs du_D/dt=200 V/µs	
Qrr	Recovered charge	µC	60	Tvj=125°C, I_{TM}=400 A di_R/dt=50 A/µs, U_R=100V	
trr	Reverse recovery time	µs	1,85		
Irrm	Peak reverse recovery current	A	65		
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	V/µs	500 1000	Tvj=125°C, U_D = 0,67 U_{DRM} Gate open	
Rthjc	Thermal resistance junction to case	°C/W	0,04	Direct current, double side cooled	

ORDERING									
	TFI	**133**	**S**	**400**	**10**	**7**	**C4**	**3**	
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	

1. Fast thyristor with interdigitated gate structure.
2. Design version.
3. Strong distributed amplified gate
4. Mean on-state current, A.
5. Voltage code (10=1000V).
6. Critical rate of rise of off-state voltage (6 ≥ 500 V/µs, 7 ≥1000 V/µs).
7. Group of turn-off time (du_D/dt=50 V/µs, C4 ≤ 6,3µs, E4 ≤ 5µs).
8. Group of turn-on time (3 ≤ 2,5 µs).



Mounting force : 9÷12 kN
Weight : 120 grams