



TET ESTEL AS
ESTONIA

November
2016

Series
TFI143S-500

High Frequency Inverter grade
Capsule Thyristor
Type TFI143S-500

Strong distributed amplified gate
and low turn-off time thyristor for
high frequency applications to 20 kHz

Maximum mean on-state current	I_{TAV}	500 A			
Maximum repetitive peak off-state and reverse voltage	U_{DRM} U_{RRM}	800 ÷ 1200 V			
Turn-off time	t_q	6,3; 8 μs			
U_{DRM}, U_{RRM}, V	800	900	1000	1100	1200
Voltage code	8	9	10	11	12
$T_{vj}, ^\circ C$	- 60 ÷ 125				

MAXIMUM ALLOWABLE RATINGS

Symbols and parameters		Units	TFI143S-500	Conditions
I_{TAV}	Mean on-state current	A	500 830	$T_c=87^\circ C$, $T_c=55^\circ C$, 180° half-sine wave, 50 Hz
I_{TRMS}	RMS on-state current	A	785	$T_c=87^\circ C$
I_{TSM}	Surge on-state current	kA	10 11	$T_{vj}=125^\circ C$ $T_{vj}=25^\circ C$ tp=10 ms $U_R=0$
I^2t	Limiting load integral	kA^2s	500 605	$T_{vj}=125^\circ C$ $T_{vj}=25^\circ C$
U_{DRM}, U_{RRM}	Repetitive peak off-state and reverse voltage	V	800÷1200	$T_j \min \leq T_{vj} \leq T_j \max$ 180° half-sine wave, 50 Hz Gate open
U_{DSM}, U_{RSM}	Non-repetitive peak off-state and reverse voltage	V	880÷1300	$T_j \min \leq T_{vj} \leq T_j \max$ 180° half-sine wave tp=10 ms, Single pulse Gate open
(diT/dt) crit	Critical rate of rise of on-state current : non - repetitive repetitive	A/ μ s	2000 1250	$T_{vj}=125^\circ C$; $U_D=0,67 U_{DRM}$, Gate pulse : 10V,5 Ω , 1 μ s rise time, 10 μ s
U_{RGM}	Peak reverse gate voltage	V	5	$T_j \min \leq T_{vj} \leq T_j \max$
T_{stg}	Storage temperature	$^\circ C$	-60÷80	
T_{vj}	Junction temperature	$^\circ C$	-60÷125	

CHARACTERISTICS

U_{TM}	Peak on-state voltage	V	2,5	$T_{vj}=25^\circ C$, $I_{TM}=3,14 I_{TAV}$
$U_{T(To)}$	Threshold voltage	V	1,4	$T_{vj}=125^\circ C$
R_T	On-state slope resistance	m Ω	0,4	1,57 $I_{TAV} < I_T < 4,71 I_{TAV}$
I_{DRM} I_{RRM}	Repetitive peak off-state and reverse current	mA	50 50	$T_{vj}=125^\circ C$, $U_D = U_{DRM}$ $U_R = U_{RRM}$

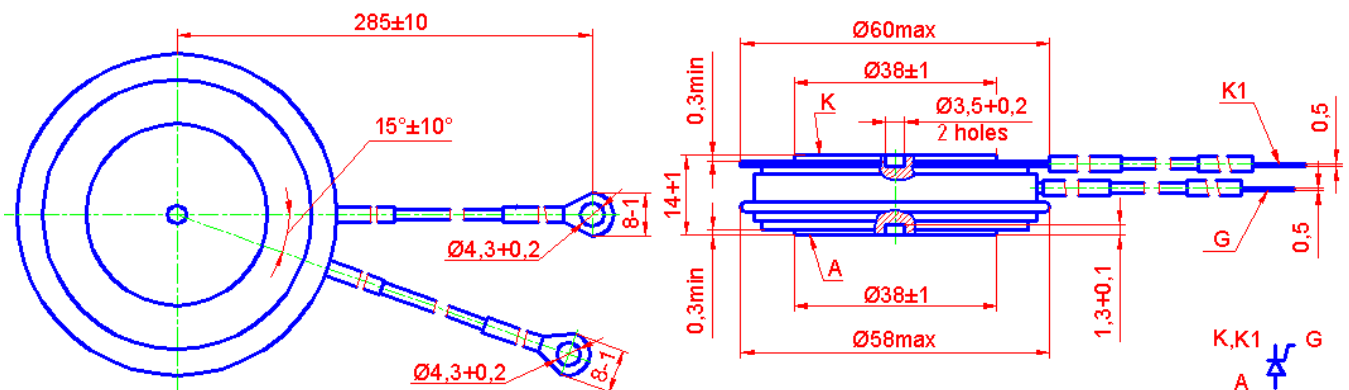
CHARACTERISTICS

Symbols and parameters		Units	TFI143S-500	Conditions
I_L	Latching current	A	16	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}$ Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
I_H	Holding current	A	0,5	$T_{vj}=25^{\circ}\text{C}, U_D=12\text{V}, \text{Gate open}$
U_{GT}	Gate trigger direct voltage	V	2,5 5,0	$T_{vj}=25^{\circ}\text{C},$ $T_{vj}=-60^{\circ}\text{C}$
I_{GT}	Gate trigger direct current	A	0,35 0,85	$T_{vj}=25^{\circ}\text{C},$ $T_{vj}=-60^{\circ}\text{C}$
U_{GD}	Gate non-trigger direct voltage	V	0,25	$T_{vj}=125^{\circ}\text{C}, U_D = 0,67 U_{DRM}$ Direct gate current
I_{GD}	Gate non-trigger direct current	mA	10	
t_{gd}	Delay time	μs	1,6	$T_{vj}=25^{\circ}\text{C}, U_D=500\text{V}$ $I_{TM} = 500 \text{ A}$
t_{gt}	Turn-on time	μs	2,5	Gate pulse : 10V, 5 Ω , 1 μs rise time, 10 μs
t_q	Turn-off time	μs	6,3; 8,0 8,0; 10,0	$T_{vj}=125^{\circ}\text{C}, I_{TM}=500 \text{ A}$ $di_R/dt = 10 \text{ A}/\mu\text{s}, U_R=100\text{V}$ $U_D = 0,67 U_{DRM}$ $du_D/dt=50 \text{ V}/\mu\text{s}$ $du_D/dt=200 \text{ V}/\mu\text{s}$
Q_{rr}	Recovered charge	μC	110	
t_{rr}	Reverse recovery time	μs	2,5	$T_{vj}=125^{\circ}\text{C}, I_{TM}=500 \text{ A}$
I_{rrM}	Peak reverse recovery current	A	88	$di_R/dt = 50 \text{ A}/\mu\text{s}, U_R=100\text{V}$
$(du_D/dt)_{crit}$	Critical rate of rise of off-state voltage	V/ μs	500 1000	$T_{vj}=125^{\circ}\text{C}, U_D = 0,67 U_{DRM}$ Gate open
R_{thjc}	Thermal resistance junction to case	$^{\circ}\text{C}/\text{W}$	0,038	Direct current, double side cooled

ORDERING

	TFI	143	S	500	10	7	C4	3	
	1	2	3	4	5	6	7	8	

- Fast thyristor with interdigitated gate structure.
- Design version.
- Strong distributed amplified gate.
- Mean on-state current, A.
- Voltage code (10=1000 V).
- Critical rate of rise of off-state voltage (6 \geq 500 V/ μs , 7 \geq 1000 V/ μs).
- Group of turn-off time ($du_D/dt=50 \text{ V}/\mu\text{s}$, 9 \leq 8 μs , C4 \leq 6,3 μs).
- Group of turn-on time (3 \leq 2,5 μs).



Mounting force : 13÷19 kN

Weight : 210 grams